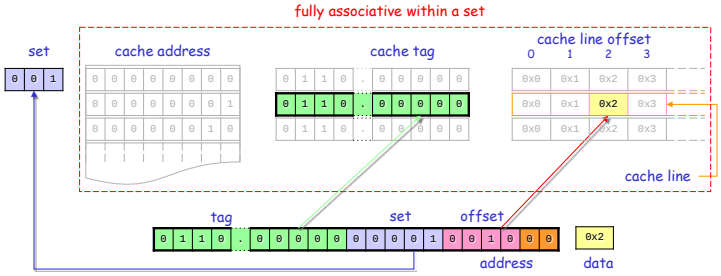
DSP Memory Architectures

DSP training

Benefits

- Estimate memory access needs
- Understand DSP memory architectures
- Understand cache architectures
- Learn to code for memory efficiency



DSP Memory Architectures

DSP is very affected by the system memory and cache architecture, yet this is often neglected in DSP teaching. To be able to program efficiently for memory you need to understand how to analyze memory access behavior of an application, and adapt that to the particular memory architecture you are using.

Class aims

We show how you can analyze the memory access behavior of a DSP application, how the memory and cache architecture affects performance, and how you can change code to use memory and cache more efficiently.

Class topics

The class explains how memory access behavior affects the performance of a program, how different memory and cache architectures are designed to be efficient when used in specific ways, and how to transform code to exploit these architectures.

- Memory access behavior
- DSP memory architectures
- Harvard and ‘super’ Harvard
- Cache
- Cache architectures
- Cache optimization

Memory accesses

How to analyze the memory access behavior of an application or program.

- Operands and operations
- Memory access patterns

DSP memory architectures

Typical DSP memory architectures.

- Register-based processing
- RISC memory architectures
- DSP memory architectures
- Harvard memory
- ‘Super’ Harvard memory

Cache

How and why cache works, cache architectures and caching strategies.

- Memory hierarchy
- Caching
- Cache misses
- Cache architectures
- Direct Mapped Cache
- Associative Cache
- Set Associative Cache
- Cache Ways
- Pre-fetching

Optimization

How to adapt code to exploit the memory and cache architecture of particular systems.

- Cache optimization
- Ordering memory accesses
- Packing data
- Dimension re-indexing
- Restricted pointers
- Register variables
- Software pipelining

Target audience

This class is aimed at programmers. engineers and managers designing products which will use DSP, and who wish to adopt more advanced strategies to use memory most efficiently.

Time and arrangements

This class takes 1 day. Check our schedule at:

www.bores.com/index_schedule.htm

It can also be presented ‘on site by special arrangement and the material can be adapted if you have specific needs.

Booking and questions

Call us by phone or send an email to book or to ask questions:

- contact Dr Chris Bore
- mobile +44 7921 153219
- email: chris@bores.com

About Us

BORES Signal Processing train managers, engineers and programmers to understand and use DSP and streaming media processing.

- established 24 years
- excellent reputation
- worldwide activities
- • www.bores.com

Bores Signal Processing Fordwater Pond Road Woking Surrey GU22 0JZ UK
Tel: +44 1483 740138 Email: chris@bores.com Web: www.bores.com